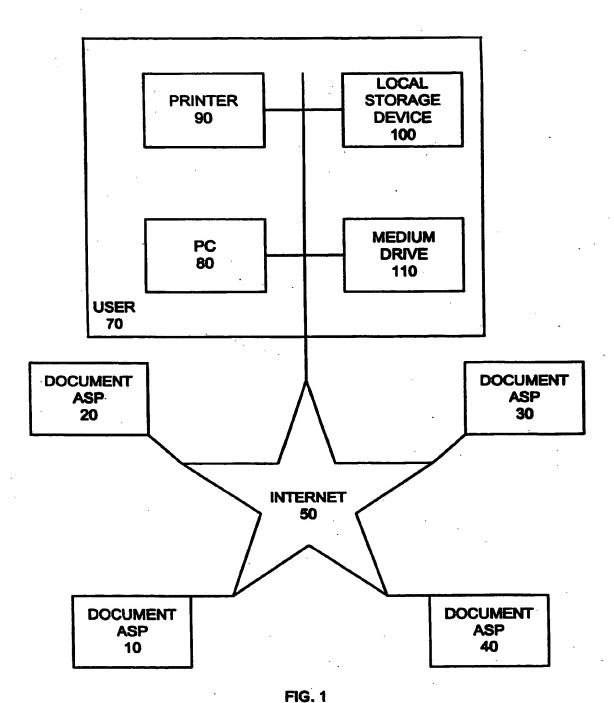
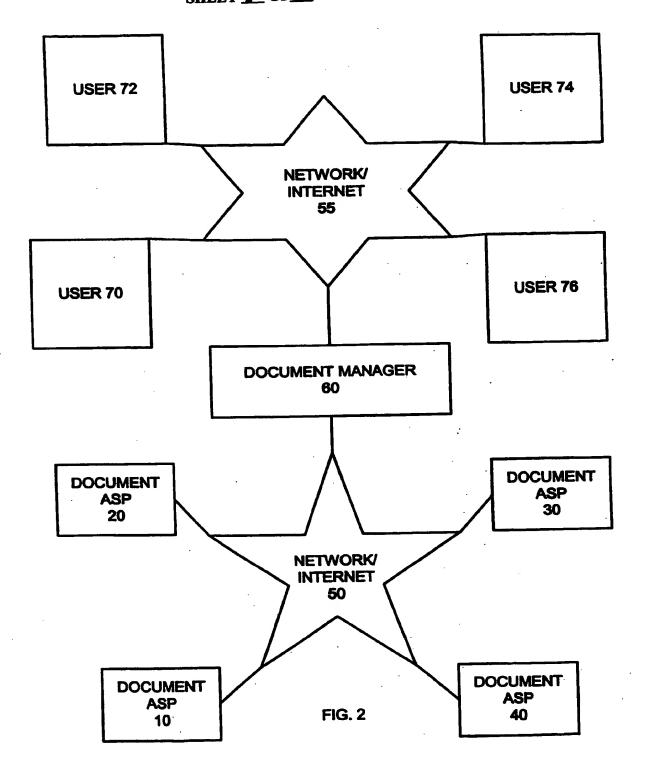
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PRIOR ART

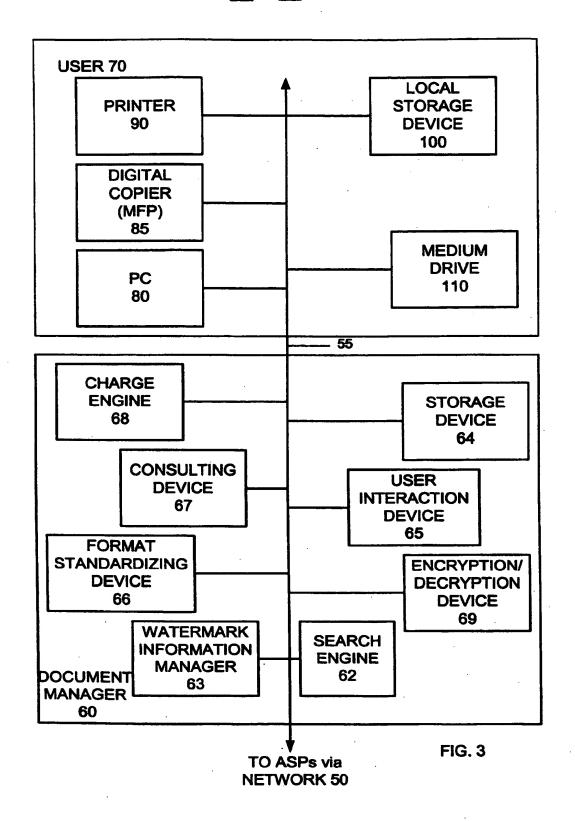
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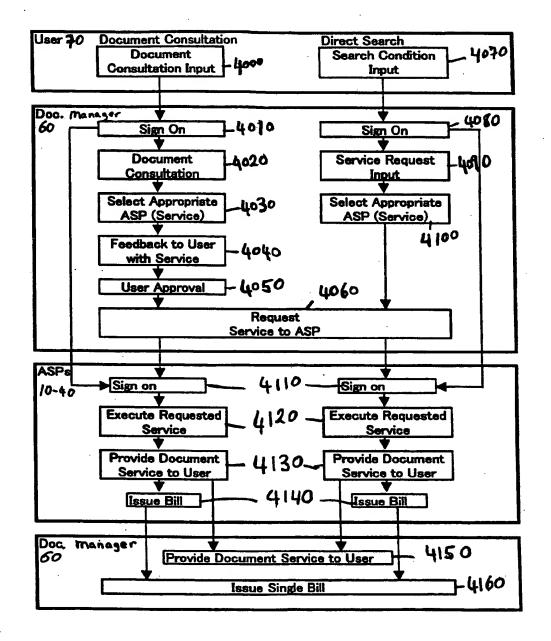
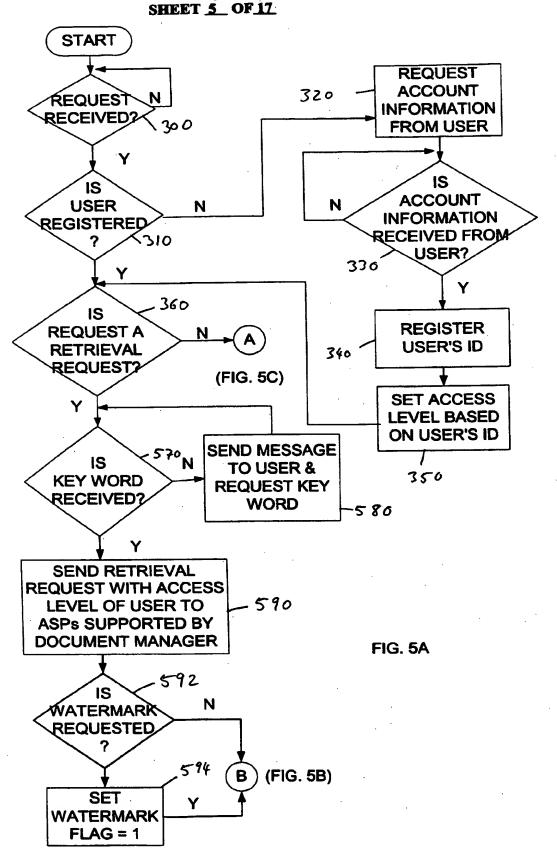


FIG.4

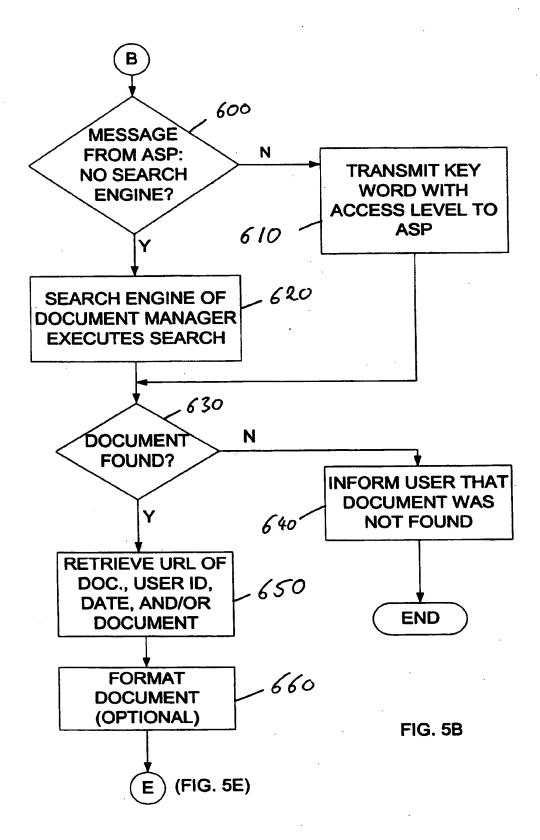
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DOCKET #:200520US-28X
INV: Shogo HYAKUTAKE, et al

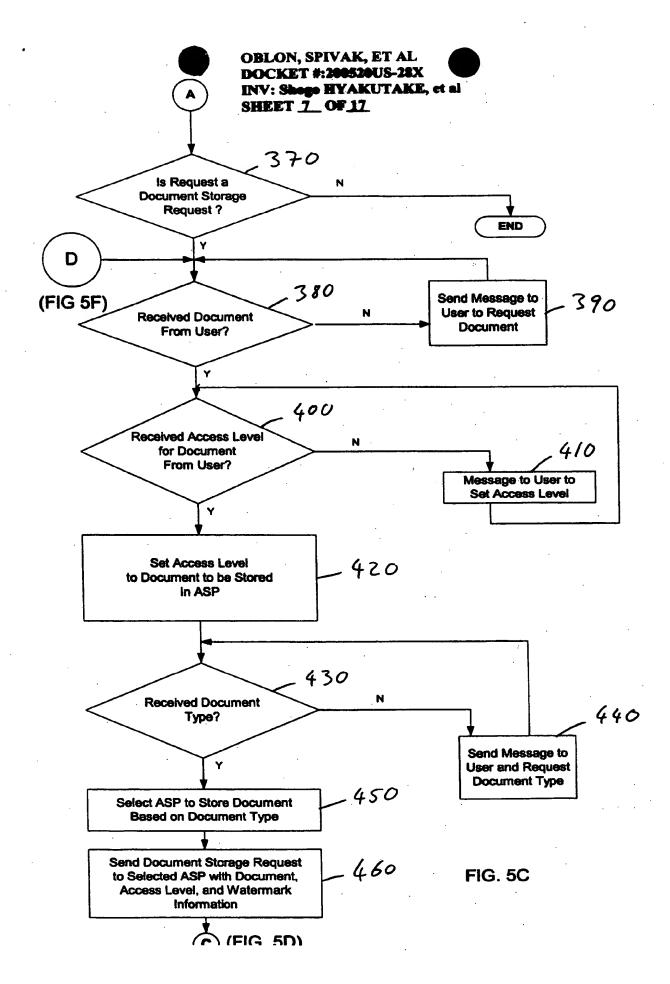


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INV: Shogo HYAKUTAKE, et al

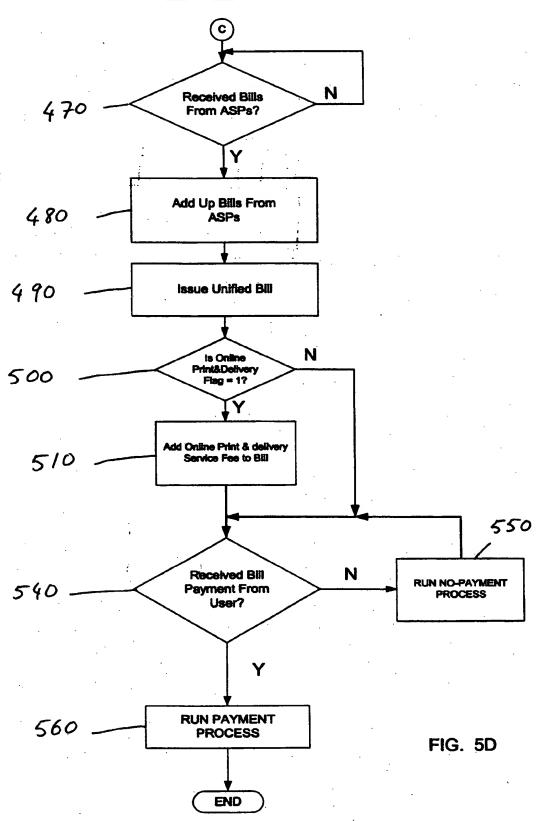
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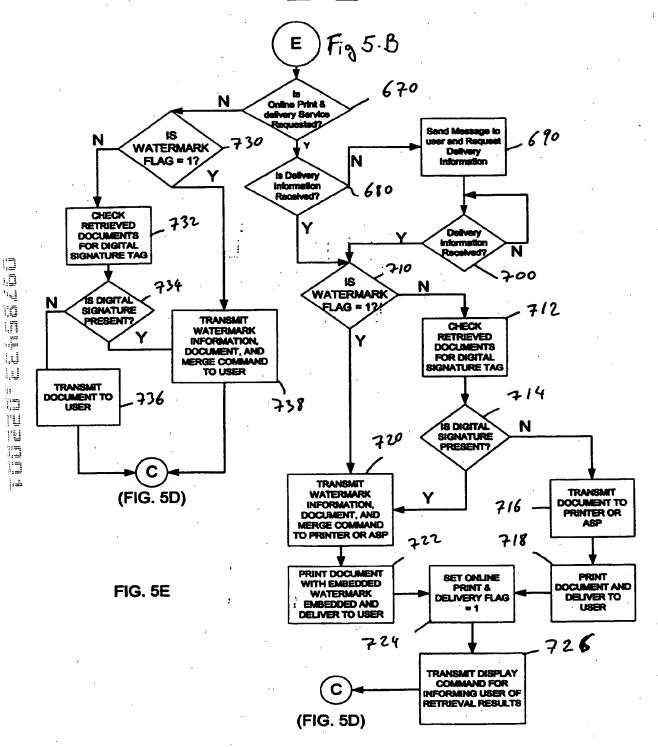
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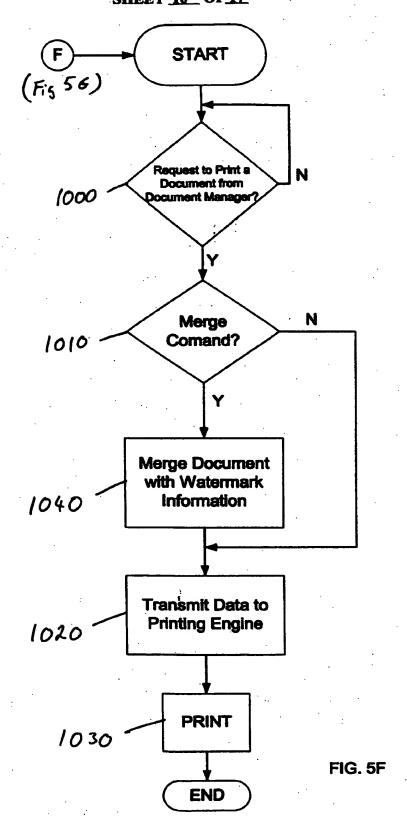


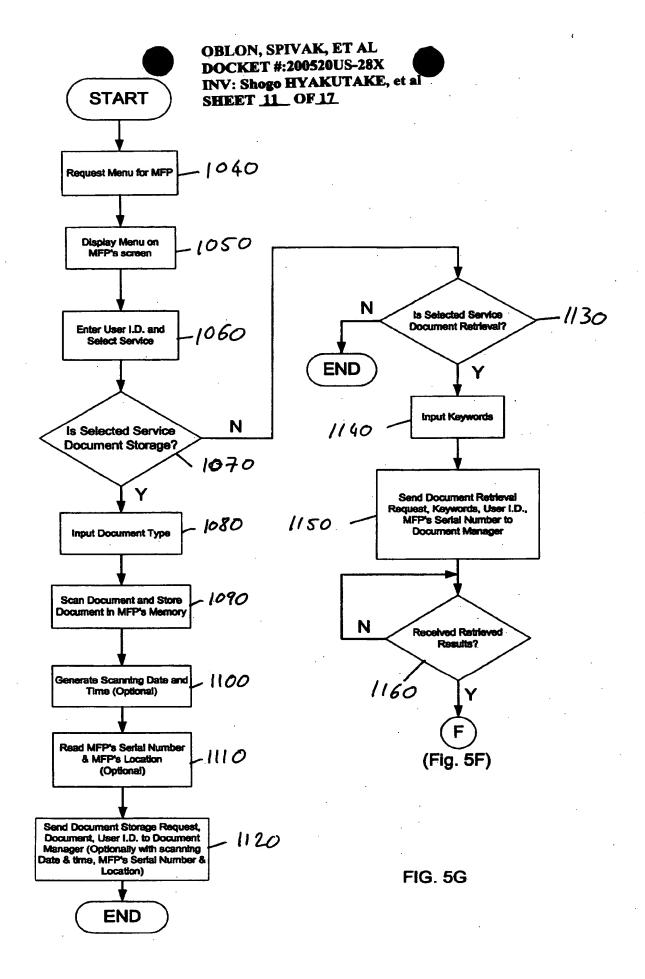
#### DBLON, SPIVAK, ET AL DOCKET #:200520US-28X INV: Shogo HYAKUTAKE, et al

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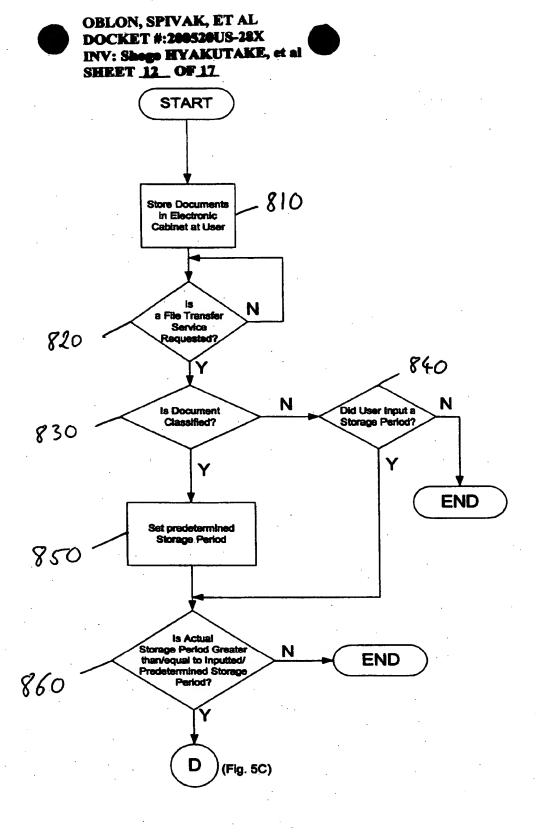
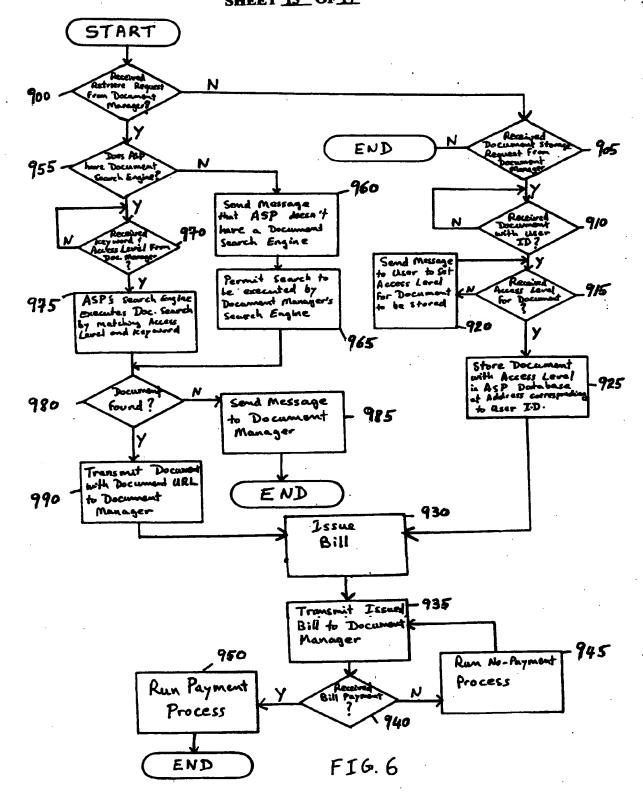


FIG. 5H

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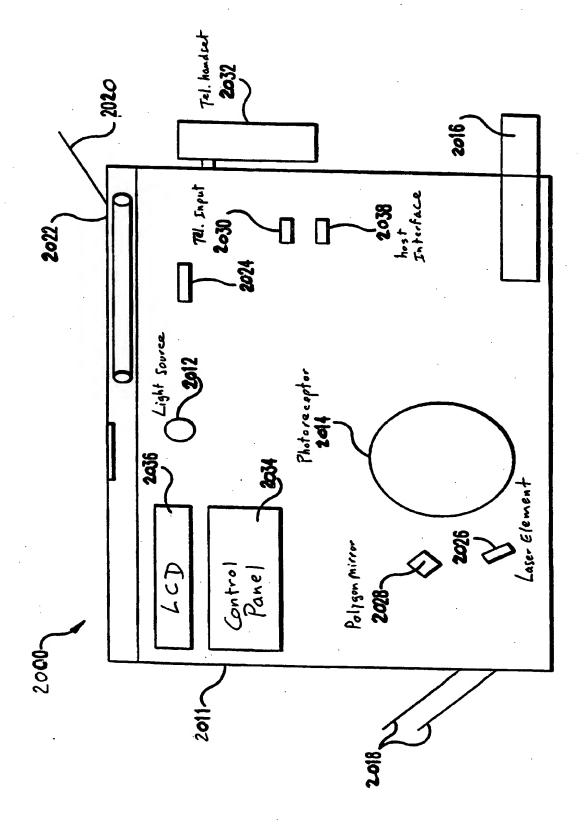
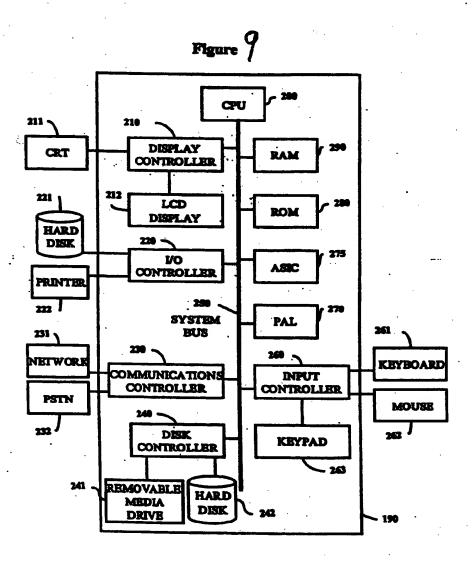


FIG. 7

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2040 2042. 2066 CPU **PRINTER** 1/F DRAM 2046 EEPROM ALU 2048 2076 **2050** ROM SCANNER 2052 I/F I/F CONTROL PANEL CONTROLLER 2054 2068 2070 I/F HOST COMPUTER CONTROLLER 2 SYSTEM 2060 **256** CONTROLLER I/F 2014 FAX/TELEPHONE CONTROLLER 3 2058 **PROCESSOR** DRAM STORAGE **STORAGE** DEVICE I/F DMA... CONTROLLER MERGE & **ANSWERING** ROUTE UNIT 2100 2072 2664 IMAGE DENSITY 2063 2>62 ADJUSTER FIG. 8

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